IN THE CLAIMS

The following is a listing of the claims of the present application:

1. (Currently Amended) An amplifier, comprising:

at least one signal amplifying transistor, coupled between an input terminal and an output terminal associated with the amplifier, for amplifying a received input signal; and

a bypass switch, coupled to the at least one signal amplifying transistor, for providing a gain mode operation and a bypass mode operation, the bypass switch comprising two transistors;

wherein in the gain mode operation, the two transistors of the bypass switch are off and the at least one signal amplifying transistor amplifies the received input signal and passes the amplified signal to the output terminal;

further wherein in the bypass mode operation, the two transistors of the bypass switch are on, a series output matching element is shorted, the at least one signal amplifying transistor is turned off, and the received input signal is passed directly from the input terminal to the output terminal.

2. (Original) The amplifier of claim 1, further comprising a controller, coupled to the at least one signal amplifying transistor, for controlling selection of gain mode and bypass mode operations.

3. (Original) The amplifier of claim 2, wherein the controller is turned off during the bypass mode operation.

4. (Original) The amplifier of claim 1, further comprising an inductor coupled between an emitter terminal of the at least one signal amplifying transistor and ground.

5. (Original) The amplifier of claim 1, further comprising an output impedance matching network coupled to the at least one signal amplifying transistor and the output terminal.

6. (Original) The amplifier of claim 1, further comprising an input impedance matching network coupled to the at least one signal amplifying transistor and the input terminal.

7. (Original) The amplifier of claim 1, wherein supply power to the bypass switch is turned off during the bypass mode operation.

8. (Currently Amended) ~~The amplifier of claim 1,~~ An amplifier, comprising:

at least one signal amplifying transistor, coupled between an input terminal and an output terminal associated with the amplifier, for amplifying a received input signal; and

a bypass switch, coupled to the at least one signal amplifying transistor, for providing a gain mode operation and a bypass mode operation, the bypass switch comprising two transistors;

wherein in the gain mode operation, the two transistors of the bypass switch are off and the at least one signal amplifying transistor amplifies the received input signal and passes the amplified signal to the output terminal;

wherein in the bypass mode operation, the two transistors of the bypass switch are on, the at least one signal amplifying transistor is turned off, and the received input signal is passed directly from the input terminal to the output terminal;

wherein respective gate terminals of the two transistors of the bypass switch are coupled to each another, wherein a source terminal of one of the two transistors is coupled to a drain terminal of the other of the two transistors and to the output terminal of the amplifier, wherein a drain terminal of one of the two transistors is coupled to the input terminal of the amplifier, and wherein a source terminal of the other of the two transistors is coupled to a collector terminal of the at least one signal amplifying transistor.

9. (Original) The amplifier of claim 1, wherein the amplifier is implemented in BiCMOS and technology.

10. (Original) The amplifier of claim 1, wherein the amplifier is implemented in CMOS technology.

11. (Currently Amended) An amplifier, comprising:

a cascode transistor pair, coupled between an input terminal and an output terminal associated with the amplifier, for amplifying a received input signal; and

a bypass switch, coupled to the cascode transistor pair, for providing a gain mode operation and a bypass mode operation, the bypass switch comprising two transistors;

wherein in the gain mode operation, the two transistors of the bypass switch are off and the cascode transistor pair amplifies the received input signal and passes the amplified signal to the output terminal;

further wherein in the bypass mode operation, the two transistors of the bypass switch are on, a series output matching element is shorted, the cascode transistor pair is turned off, and the received input signal is passed directly from the input terminal to the output terminal.

12. (Original) An amplifier, comprising:

at least one signal amplifying transistor, coupled between an input terminal and an output terminal associated with the amplifier, for amplifying a received input signal;

a bypass switch, coupled to the at least one signal amplifying transistor, for providing a gain mode operation and a bypass mode operation; and

an output impedance matching network, coupled to the at least one signal amplifying transistor and the output terminal; wherein in the gain mode operation, the bypass switch is inactive and the at least one signal amplifying transistor amplifies the received input signal and passes the amplified signal to the output terminal;

further wherein in the bypass mode operation, the bypass switch is active, the at least one signal amplifying transistor is turned off, the received input signal is passed directly from the input terminal to the output terminal, and a load impedance is not modified by the output impedance matching network.

13. (Currently Amended) A communications receiver, comprising:

a low-noise amplifier having an input terminal and an output terminal, the low-noise amplifier comprising:

at least one signal amplifying transistor, coupled between an input terminal and an output terminal associated with the low-noise amplifier, for amplifying a received input signal; and

the at least one signal amplifying transistor, for providing a gain mode operation and a bypass mode operation, the bypass switch comprising two transistors;

wherein in the gain mode operation, the two transistors of the bypass switch are off and the at least one signal amplifying transistor amplifies the received input signal and passes the amplified signal to the output terminal;

further wherein in the bypass mode operation, the two transistors of the bypass switch are on, a series output matching element is shorted, the at least one signal amplifying transistor is turned off, and the received input signal is passed directly from the input terminal to the output terminal.

14. (Original) The communications receiver of claim 13, wherein at least a portion of the receiver is implemented an integrated circuit.

15. (Currently Amended) A method of providing a gain mode operation and a bypass mode operation in a low-noise amplifier, comprising the steps of:

configuring the low-noise amplifier to comprise: (i) at least one signal amplifying transistor, coupled between an input terminal and an output terminal associated with the amplifier, for amplifying a received input signal; and (ii) a bypass switch, coupled to the at least one signal amplifying transistor, for providing a gain mode operation and a bypass mode operation, the bypass switch comprising two transistors;

in the gain mode operation, turning off the two transistors of the bypass switch and amplifying the received input signal with the at least one signal amplifying transistor, and passing the amplified signal to the output terminal;

in the bypass mode operation, turning on the two transistors of the bypass switch, shorting a series output matching element, turning off the at least one signal amplifying transistor, and directly passing the received input signal from the input terminal to the output terminal.